

WHAT IS CLAIMED IS:

- Sub
A1
1. An active matrix device comprising an array of picture elements, each of which comprises an image element, a first charge storage element connected to the image element, and a first semiconductor switch for connecting a data line to the first charge storage element and the image element, characterised in that each picture element comprises a second charge storage element and a second semiconductor switch switchable independently of the first switch to connect the second charge storage element to the first charge storage element and the image element so as to increase the charge storage capacity.
 2. A device as claimed in claim 1, characterised in that each image element is a light modulating element.
 3. A device as claimed in claim 2, characterised in that each image element is transmissive.
 4. A device as claimed in claim 2, characterised in that each image element is reflective.
 5. A device as claimed in claim 2, characterised in that

each image element is a liquid crystal element.

6. A device as claimed in claim 1, characterised in that each image element is a light emitting element.

7. A device as claimed in claim 1, characterised in that each of the first and second switches is a thin film transistor.

8. A device as claimed in claim 1, characterised in that the charge storage capacity of the second charge storage element is greater than that of the first charge storage element.

9. A device as claimed in claim 1, characterised in that, for each picture element, the second charge storage element and the second switch are connected in series across the first charge storage element.

10. A device as claimed in claim 1, characterised in that the picture elements are arranged as rows and columns with the picture elements of each column being connected to a respective data line and the picture elements of each row being connected to a respective scan line.

Sub
A1
Cont

RECEIVED

11. A device as claimed in claim 10, characterised in that the second switches of each row of picture elements have control terminals connected to a respective control line.

12. A device as claimed in claim 11, characterised in that the control lines are connected together.

13. A device as claimed in claim 1, characterised in that, for each picture element, the second switch has a control terminal connected to first terminals of the first and second charge storage elements.

14. A device as claimed in claim 10, characterised in that the first and second charge storage elements of each row of picture elements have first terminals connected to a respective common line.

15. A device as claimed in claim 10, characterised in that the first and second charge storage elements of each adjacent pair of rows of picture elements have first terminals connected to a respective common line.

16. A device as claimed in claim 10, characterised in that

Sub
A1
Cont

the first and second charge storage elements of each row of picture elements have first terminals connected to the scan line of an adjacent row.

17. A device as claimed in claim 1, characterised in that the first and second charge storage elements of each picture element comprise first and second capacitors, respectively.

18. A device as claimed in claim 17, characterised in that the first and second capacitors of each picture element have a common plate.

19. A device as claimed in claim 18, characterised in that the common plate comprises a part of a gate metal interconnect layer (GL).

20. A device as claimed in claim 19, characterised in that the first capacitor of each picture element has a further plate comprising part of a source metal interconnect layer (SL).

21. A device as claimed in claim 19, characterised in that the second capacitor of each picture element has a further

Sub
A1
cont

11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

plate comprising part of a heavily doped silicon layer.

22. A device as claimed in claim 17, characterised in that the second capacitor of each picture element has a dielectric comprising gate oxide.

23. A device as claimed in claim 22, characterised in that the second capacitor of each picture element comprises a metal oxide silicon capacitor.

24. A device as claimed in claim 23, characterised in that the metal oxide silicon capacitor forms the second switch and has source and drain terminals connected to the first switch and the image element.

25. A device as claimed in claim 23, characterised in that the first capacitor of each picture element comprises the gate/source overlap capacitance and the gate/drain overlap capacitance of the metal oxide silicon capacitor.

26. A device as claimed in claim 25, characterised in that the metal oxide silicon capacitor (35) has a lightly doped drain below the gate electrode.

Sub
AI
Cmt

27. A display characterised by comprising a device as claimed in claim 1.

Sub
AI
end

RECEIVED